Amendments to the Claims:

1. (Currently Amended) A semiconductor package comprising:

a single non-conductive film layer defining opposed top and bottom film surfaces and a peripheral edge, the film layer including a plurality of vias disposed therein;

a plurality of upper leads disposed on the top film surface adjacent respective ones of the vias;

a plurality of lower leads disposed on the bottom film surface adjacent respective ones of the vias, each of the lower leads being electrically connected to a respective one of the upper leads;

at least one transmission line element disposed on the top film surface and electrically connected to at least one of the upper leads;

at least one semiconductor die attached to the top film surface and electrically connected to at least one of the upper leads and the transmission line element; and

a package body disposed on the film layer and extending to the peripheral edge thereof, the package body ~~covering~~ **encapsulating** the semiconductor die, the upper leads, **and** the transmission line element, and **being adhered to** the top film surface.

2. (Original) The semiconductor package of Claim 1 comprising a plurality of transmission line elements disposed on the top film surface, the semiconductor die being electrically connected to at least one of the transmission line elements.

3. (Original) The semiconductor package of Claim 2 wherein the transmission line elements are selected from the group consisting of:

an inductor;

a shortwave coupler;

a balun;

a filter; and

combinations thereof.

4. (Original) The semiconductor package of Claim 1 wherein the upper and lower leads and the transmission line element each include a nickel/gold layer plated thereon.

5. (Original) The semiconductor package of Claim 1 wherein the semiconductor die is electrically connected to the upper lead and to the transmission line element by respective ones of a plurality of bond wires which are each covered by the package body.

6. (Original) The semiconductor package of Claim 5 wherein at least some of the upper leads each include a conductive trace connected thereto and extending therefrom, the bond wires being used to electrically connect the semiconductor die to at least one of the traces.

7. (Original) The semiconductor package of Claim 1 further comprising a plurality of pads disposed on the top film surface and electrically connected to respective ones of the upper leads, the pads being arranged in at least one set which is configured to accommodate a passive device.

8. (Original) The semiconductor package of Claim 7 wherein the pads are arranged in multiple sets, each of the sets being configured to accommodate a passive device.

9. (Original) The semiconductor package of Claim 1 wherein the vias are segregated into an outer set which extends along and in relative close proximity to a peripheral edge of the non-conductive sheet, and an inner set which is disposed within the outer set.

10. (Original) The semiconductor package of Claim 1 wherein the non-conductive sheet is fabricated from a polyimide film.

11. (Original) The semiconductor package of Claim 1 wherein each of the vias is lined with a conductive metal material to facilitate the electrical connection of the upper leads to respective ones of the lower leads.

12. (Original) The semiconductor package of Claim 1 wherein each of the vias is filled with a conductive metal material to facilitate the electrical connection of the upper leads to respective ones of the lower leads.

13. (Currently Amended) A ~~substrate for integration into a~~ semiconductor package, ~~the substrate~~ comprising:

a single non-conductive film layer defining opposed top and bottom **film** surfaces and **a plurality of peripheral film side surfaces, the film layer** including a plurality of vias disposed therein;

a plurality of upper leads disposed on the top film surface adjacent respective ones of the vias;

a plurality of lower leads disposed on the bottom film surface adjacent respective ones of the vias, each of the lower leads being electrically connected to a respective one of the upper leads; ~~and~~

a plurality of transmission line elements disposed on the top film surface and electrically connected to at least one of the upper leads**; and**

a package body encapsulating the upper leads and the transmission line elements, the package body being disposed on the top film surface and defining a plurality of generally vertical body side surfaces which are substantially coplanar with respective ones of the film side surfaces.

14. (Currently Amended) The ~~substrate~~ **semiconductor package** of Claim 13 wherein the transmission line elements are selected from the group consisting of:

an inductor;

a shortwave coupler;

a balun;

a filter; and

combinations thereof.

15. (Cancelled)

16. (Currently Amended) The ~~substrate~~ **semiconductor package** of Claim 13 further comprising a plurality of pads disposed on the top film surface and electrically connected to respective ones of the upper leads, the pads being arranged in at least one set which is configured to accommodate a passive device.

17. (Currently Amended) The ~~substrate~~ **semiconductor package** of Claim 16 wherein the pads are arranged in multiple sets, each of the sets being configured to accommodate a passive device.

18. (Currently Amended) The ~~substrate~~ **semiconductor package** of Claim 13 wherein the vias are segregated into an outer set which extends along and in relative close proximity to ~~a~~ **the** peripheral edge of the ~~non-conductive sheet~~ **film layer**, and an inner set which is disposed within the outer set.

19. (Currently Amended) The ~~substrate~~ **semiconductor package** of Claim 13 wherein each of the vias is lined with a conductive metal material to facilitate the electrical connection of the upper leads to respective ones of the lower leads.

20. (Currently Amended) The ~~substrate~~ **semiconductor package** of Claim 13 wherein each of the vias is filled with a conductive metal material to facilitate the electrical connection of the upper leads to respective ones of the lower leads.

21. (New) A semiconductor package comprising:

a single non-conductive film layer defining opposed top and bottom film surfaces and a plurality of peripheral film side surfaces which extend generally perpendicularly between the top and bottom film surfaces;

a plurality of upper leads disposed on the top film surface;

a plurality of lower leads disposed on the bottom film surface, the film layer including means for electrically connecting each of the lower leads to a respective one of the upper leads;

at least one transmission line element disposed on the top film surface and electrically connected to at least one of the upper leads;

at least one semiconductor die attached to the top film surface and electrically connected to at least one of the upper leads and the transmission line element; and

a package body encapsulating the semiconductor die, the upper leads and the transmission line element, the package body being disposed on the top film surface and defining a plurality of generally vertical body side surfaces and a

generally horizontal body top surface which is substantially orthogonal to the body side surfaces.